REMARKS

Claims 25, 26, 31-34, 37- 40, and 43-49 are rejected in the outstanding Office Action under 35 U.S.C. § 112, 35 U.S.C. § 103(a), or 35 U.S.C. § 132. Applicants have amended claims 25, 33, 38, 39, 44-49, and, after careful consideration of the teachings of the references cited in the Office Action, applicants respectfully submit that claims 25, 26, 31-34, 37- 40, and 43-49 recite subject matter which is novel and nonobvious in light of the references cited in the Office Action.

Entry of Amendments

The amendments to the claims are supported by the as-filed application, and entry thereof is respectfully solicited. No new matter has been added.

35 U.S.C. § 132 Objection to Amendment

The amendments filed November 28, 2000 and October 15, 2001 stand objected to under 35 U.S.C. § 132 for allegedly introducing new matter into the disclosure. The examiner states that the elements "free of field oxide [structures]" and "said substantially dopant-free, uninterrupted diffusion barrier layer [having] a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure" are new matter. Applicants have amended independent claims 25, 33, 39, and 46 to remove the latter element, thereby rendering moot the objection to this element. Applicants respectfully traverse the objection as to the element "free of field oxide [structures]," as hereinafter set forth.

Applicants submit that the term "free of field oxide [structures]" is supported by both the specification and drawings of the as-filed application and, therefore is not new matter because any "information contained in any one of the specification, claims, or drawings of the application as filed may be added to any other part of the application without introducing new matter." M.P.E.P. § 2163.06.

The as-filed specification discloses that the diffusion barrier layer is deposited on both surfaces of the semiconductor substrate to encapsulate the substrate. Page 7, lines 8-28. The encapsulated structure is then annealed to activate areas on the semiconductor substrate. Page 8, lines 1-4. Subsequently, field oxide structures are grown on the first surface of the semiconductor substrate. Since these field oxide structures are grown on the semiconductor substrate after the intermediate structure is annealed, the field oxide structures are necessarily not present on the semiconductor substrate until after the intermediate structure is annealed. This conclusion is further supported by statements in the specification that annealing the semiconductor substrate before the field oxide structures are grown reduces encroachment of the field oxide structures and that formation of the encapsulated structure before annealing eliminates contamination and damage to temperature sensitive portions of the semiconductor device. Page 6, lines 4-9; page 8, lines 9-15. Therefore, the intermediate structure comprises a semiconductor substrate that does not have field oxide structures and is "free of field oxide [structures]."

The drawings also provide support for the term "free of field oxide structures," which is best shown by reference to FIGs. 1-3 (intermediate structure before annealing) and FIGs. 7-8 (intermediate structure after annealing). The intermediate structure shown in FIGs. 1-3 comprises, among other things, a semiconductor substrate having a first and second surface, n-wells, p-wells, a pad oxide film, and a diffusion barrier layer. In contrast, as illustrated in FIGs. 7 and 8, the intermediate structure comprises field oxide structures, which are grown on the first surface of the semiconductor substrate after the high temperature anneal.

Applicants respectfully submit that the drawings may be relied on as support for the term "free of field oxide [structures]" because the drawings illustrate the absence of field oxide structures in FIGs. 1-3 and the presence of that element in FIGs. 7-8. By rejecting this element as new matter, when a comparison of the drawings shows that the semiconductor substrate is free of field oxide structures until after annealing, the examiner is in effect requiring applicants to explicitly describe elements that are not present in their claimed invention. Since the drawings

are not relied on to support the scale of an illustrated element, the examiner's statement that the drawings may not be relied on because they are not drawn to scale is inapplicable.

Since the as-filed specification and drawings disclose that the field oxide structures are not present until after annealing, the semiconductor substrate is "free of field oxide structures" and the as-filed disclosure supports this element. Therefore, applicants respectfully request this is not new matter and that the objection be withdrawn.

35 U.S.C. § 112 Claim Rejections

35 U.S.C. § 112, ¶1

Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected under 35 U.S.C. § 112, ¶1, as assertedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The examiner states that there is no written description for the terms "free of field oxide [structures]" and "said substantially dopant-free, uninterrupted diffusion barrier layer [having] a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure." Applicants have deleted the latter element, thereby rendering moot the rejections based on that element.

Applicants respectfully traverse the rejection as to the term "free of field oxide [structures]" because, as discussed in detail in the 35 U.S.C. § 132 objections, the as-filed specification provides adequate written description that the semiconductor substrate is free of field oxide structures.

35 U.S.C. § 112, ¶2

Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected under 35 U.S.C. § 112, ¶2, as allegedly failing to set forth the subject matter that applicants regard as their invention. Applicants have amended claims 25, 33, 39, and 46 so that the preamble and the elements

defined in the claims are consistent in scope. Therefore, applicants request that this rejection be withdrawn.

Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected under 35 U.S.C. § 112, ¶2, as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Applicants have amended claims 25, 33, 39, and 46 to clarify that the invention is an annealed intermediate structure. Therefore, this rejection should be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 25, 26, 31, 33, 34, 37-40, and 43-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,545,577 issued to Tada ("Tada") in view of U.S. Patent No. 5,874,325 issued to Koike ("Koike"). Claims 32 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tada and Koike, as applied to claims 25 and 46, and further in view of U.S. Patent No. 5,846,596 issued to Shim et al. ("Shim").

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The examiner bears the burden of establishing that each of these three criteria has been met. If one of these criteria is not met, the examiner has not established a *prima facie* case of obviousness.

Obviousness Rejection Based on Tada in View of Koike

Claims 25, 26, 31, 33, 34, 37-40, and 43-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tada in view of Koike. Applicants respectfully submit that a *prima facie* case of obviousness has not been established because Tada and Koike do not teach or suggest all the limitations of the claimed invention.

As amended, independent claim 25 recites an intermediate structure in the formation of an isolation structure that, among other things, includes a semiconductor substrate that is free of field oxide structures and has a first and a second opposing surface. The semiconductor substrate has p-wells and n-wells on its first surface. The p-wells comprise at least one activated, annealed n-type area and the n-wells comprise at least one activated, annealed p-type area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate.

In contrast, Tada discloses a method of producing a semiconductor device that has two MIS transistor circuits on a first surface of the device. A silicon nitride layer is used as a mask to form a field oxide film on the first surface of the semiconductor substrate. Column 6, lines 27-31. As a result, gate oxides of different thicknesses are produced without contacting the resist layer, thus reducing contamination due to the resist. Column 8, line 48-column 9, line 9.

Koike discloses a method of manufacturing a semiconductor device that includes a gettering layer. The gettering layer is comprised of a silicon thin film to which impurities have been added. Column 1, lines 53-56. The silicon thin film is applied to both surfaces of a semiconductor substrate. Column 6, line 56-column 7, line 2. Silicon nitride layers are then deposited over the silicon thin films to protect the gettering properties of the silicon thin film layers until the manufacturing process is complete. Column 6, line 56-Column 7, line 25.

Applicants respectfully submit that Tada does not teach or suggest all the limitations of independent claim 25. Specifically, Tada does not teach or suggest the following limitations. As acknowledged by the examiner, Tada does not disclose a substantially dopant-free, uninterrupted

barrier layer that extends over the second surface of the substrate. Office Action of December 19, 2001, page 6. In addition, since Tada does not disclose that the barrier layer extends over the second surface of the substrate, Tada also does not disclose that the intermediate structure is encapsulated. Tada also does not disclose that the p-wells and n-wells comprise activated, annealed n-type and p-type areas, respectively.

While Koike disclose that its silicon nitride layer extends over both the first and second surfaces of the substrate, Koike does not disclose p-wells and n-wells on the first surface of the substrate or activated, annealed n-type and p-type areas within the p-wells and n-wells, respectively.

In summary, neither Tada nor Koike discloses that p-wells and n-wells on the first surface of the substrate comprise activated, annealed n-type and p-type areas, respectively. Therefore, a *prima facie* case of obviousness has not been established because the cited references do not teach or suggest all the limitations of independent claim 25. Therefore, applicants respectfully request that the rejection of claim 25 be withdrawn.

Dependent claims 26 and 31 include all of the claim limitations of claim 25 and, therefore, are allowable as depending from an allowable claim.

With regard to independent claims 33, 39, and 46, applicants respectfully submit that a *prima facie* case of obviousness has not been established for the same reason discussed above with regard to claim 25. Namely, the cited references do not teach or suggest all the claim limitations.

As amended, independent claims 33 recites an intermediate structure in the formation of an isolation structure that includes, among other things, a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The semiconductor substrate has at least one p-well and at least one n-well on its first surface. The p-wells and n-wells comprise at least one activated, annealed doped area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate.

As amended, claim 39 recites an intermediate structure in the formation of an isolation structure that includes, among other things, a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The first surface of the substrate comprises at least one activated, annealed first doped area, which has at least one activated, annealed second, differently doped area within the first doped area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate.

As amended, claim 46 recites an intermediate structure in the formation of an isolation structure that includes, among other things, a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The substrate comprises p-wells and n-wells on its first surface, with activated, annealed n-type areas and p-type areas within the wells. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer that extends over both the first and second surfaces of the substrate.

As previously discussed, Tada and Koike do not disclose that the p-wells and n-wells on the first surface of the semiconductor substrate comprise activated, annealed n-type and p-type (or doped) areas, respectively. Therefore, a *prima facie* case of obviousness of claims 33, 39, and 46 has not been established and applicants respectfully request that the rejection of claims 33, 39, and 46 be withdrawn.

Dependent claims 34, 37, and 38 include all of the claim limitations of claim 33 and, therefore, are allowable as depending from an allowable claim. Dependent claims 40 and 43-45 include all of the claim limitations of claim 39 and, therefore, are allowable as depending from an allowable claim. Dependent claims 47 and 48 include all of the claim limitations of claim 46 and, therefore, are allowable as depending from an allowable claim.

Applicants have amended independent claims 25, 33, 39, and 46 to remove the term "said substantially dopant-free, uninterrupted diffusion barrier layer [having] a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-

anneal intermediate structure," which is stated by the examiner to be a product by process limitation.

Obviousness Rejection Based on Tada and Koike and Further in View of Shim

Claims 32 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tada and Koike, as applied to claims 25 and 46 above, and further in view of Shim. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claim 32 depends from claim 25, and, therefore, includes all the claim limitations of claim 25. Therefore, claim 32 recites an intermediate structure in the formation of an isolation structure that includes, among other things, a semiconductor substrate that is free of field oxide structures and has a first and a second opposing surface. The semiconductor substrate has p-wells and n-wells on its first surface. The p-wells comprise activated, annealed n-type areas and the n-wells comprise activated, annealed p-type areas. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate. This diffusion barrier layer is comprised of silicon oxynitride.

Shim discloses a method of forming field oxide isolation regions having sloped edges. Column 2, lines 5-6. In this method, a silicon nitride or silicon oxynitride layer is applied to one surface of a substrate and is used as a first oxidation resistant layer. Column 3, lines 17-19. The first oxidation resistant layer, in combination with a first pad insulation layer, is patterned to expose portions of the substrate, which are subsequently oxidized into field oxide isolation regions having sloped walls. Column 3, lines 19-67.

As previously discussed, Tada and Koike do not teach or suggest all the limitations of the claimed invention. Applicants respectfully submit that Shim also does not teach or suggest the limitation of p-wells and n-wells on the first surface of the substrate that comprise activated, annealed n-type and p-type areas, respectively.

In addition, the nonobviousness of independent claim 25 precludes the rejection of claim 32 because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See In re Fine,* 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); *see also* M.P.E.P. § 2143.03.

Since a *prima facie* case of obviousness has not been established for the reasons discussed above, applicants respectfully request that the rejection of claim 32 be withdrawn.

Claim 49 depends from independent claim 46 and, therefore, includes all the claim limitations of claim 46. Claim 49 recites an intermediate structure in the formation of an isolation structure that includes, among other things, a semiconductor substrate that is free of field oxide structures and that has first and second opposing surfaces. The substrate comprises p-wells and n-wells on its first surface, with activated, annealed n-type areas and p-type areas within the wells. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer, comprised of silicon oxynitride, that extends over both the first and second surfaces of the substrate.

Claim 49 is not obvious for the same reasons discussed in the rejection of claim 32. To reiterate, Tada and Koike do not teach or suggest all the limitations of the claimed invention. Applicants respectfully submit that Shim also does not teach or suggest the limitation of p-wells and n-wells on the first surface of the substrate that comprise activated, annealed n-type and p-type areas, respectively.

In addition, the nonobviousness of independent claim 46 precludes the rejection of claim 49, which depends from claim 46, because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See In re Fine,* 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); *see also* M.P.E.P. § 2143.03.

Since a *prima facie* case of obviousness has not been established for the reasons discussed above, applicants respectfully submit that the rejection of claim 49 be withdrawn.

CONCLUSION

Claims 25, 26, 31-34, 37- 40, and 43-49 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

25. (Six times amended) [A pre-anneal] An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one activated, annealed p-type area within said at least one n-well[;] and at least one activated, annealed n-type area within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, [wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure] said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

33. (Four times amended) [A pre-anneal] An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one activated, annealed doped area within at least one of said at least one n-well and said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, [wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal

intermediate structure] said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

38. (Amended) The structure of claim 33, wherein said at least one activated, annealed doped area comprises an impurity selected from the group consisting of an n-type impurity and a p-type impurity.

39. (Four times amended) [A pre-anneal] An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one activated, annealed first doped area on said substrate first surface;

at least one activated, annealed second, differently doped area within said at least one first doped area; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, [wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure] said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

44. (Amended) The structure of claim 39, wherein said at least one activated, annealed first doped area comprises a p-type impurity and said at least one activated, annealed second, differently doped area comprises an n-type impurity.

45. (Amended) The structure of claim 39, wherein said at least one activated, annealed first doped area comprises an n-type impurity and said at least one activated, annealed second, differently doped area comprises a p-type impurity.

46. (Twice Amended) [A pre-anneal] An intermediate structure useful in the formation of electrical device isolation structures, comprising:

a semiconductor substrate that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well defined on said first surface of said substrate;

at least one activated, annealed p-type area defined within said at least one n-well[;] and

at least one activated, annealed n-type area defined within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate[, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure].

47. (Amended) The [pre-anneal intermediate] structure of claim 46 further comprising a layer of oxide between said first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

48. (Amended) The [pre-anneal intermediate] structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon nitride.

49. (Amended) The [pre-anneal intermediate] structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.